REMARKS

Claims 1-28, 30, 46, and 47 are rejected. Claims 1, 3, 5, 7, 9, 11-14, 19, and 22-24 are amended. Claims 2, 6, 8, 15-18, 30-45, and 47 are canceled. New Claims 59-60 are added. Reconsideration and allowance of Claims 1, 3-5, 7, 9-14, 19-28, and 59-60 are respectfully requested.

Rejections under 35 USC 102

Claims 1-28, 30, and 46-47 are rejected under 35 USC 102(e) as being anticipated by U.S. Patent 6,542,391 to Pereira et al (Periera). Applicant respectfully traverses these rejections, as individually discussed below with respect to the remaining pending independent claims.

Independent Claim 1

Applicant's Claim 1 is amended to recite:

> A content addressable memory (CAM) device, comprising:
>
> a plurality of CAM array blocks each including a plurality of rows of CAM cells, wherein each CAM array block has a unique hard priority indicative of the CAM array block's physical location relative to the other CAM array blocks, and has an arbitrarily assigned soft priority that is independent of the CAM array block's physical location relative to the other CAM array blocks; and
>
> a priority resolution circuit configured to hierarchically resolve competing soft priorities between a plurality of active hit signals according to numeric significance so that a first of the plurality of active hit signals having a first soft priority will block resolution of a second of the plurality of active hit signals having a second soft priority when the first soft priority is higher than the second soft priority and vice versa when the second soft priority is higher than the first soft priority, and configured to resolve competing hard priorities between two or more of the plurality of active hit signals having equivalent highest soft priorities by identifying which of the two or more of the plurality of active hits signals has the highest hard priority.

Pereira fails to disclose or suggest the CAM device of Applicant's Claim 1.

First, Pereira does not disclose "a plurality of CAM array blocks each including a plurality of rows of CAM cells, wherein each CAM array block has a unique hard priority indicative of the CAM array block's physical location relative to the other CAM array blocks, and has an arbitrarily assigned soft priority that is independent of the CAM array block's physical location relative to the other CAM array blocks," as recited in Applicant's Claim 1.

Pereira discloses a CAM device having a plurality of CAM blocks, and teaches that if one of the CAM blocks is defective, the defective CAM block can be disabled and any remaining non-defective CAM blocks positioned at higher hard priority locations can be logically re-mapped to address spaces previously occupied by the defective CAM block. In this manner, all of the non-defective CAM blocks will have contiguous addresses, thereby increasing manufacturing yield, for example, by allowing a CAM device having 3 non-defective CAM blocks and 1 defective CAM block to be sold as a 3-block CAM device rather than discarding the CAM device (Pereira, col. 17, lines 21-33). Pereira's address re-mapping scheme is performed by selectively altering the first 2 bits of the CAM address (i.e., A[13:12] in Pereira's Fig. 9) that are used to identify one of the 2^2=4 CAM blocks 805 (Pereira, col. 17, lines 34-50). However, because Pereira's non-defective blocks are always translated into a contiguous address space, the re-mapped addresses of Pereira's CAM blocks are *always indicative of the relative physical locations of the CAM blocks*. Therefore, Pereira's re-mapped addresses cannot be *arbitrarily assigned* soft priorities that are *independent* of the CAM array block's physical location relative to the other CAM array blocks, as recited in Applicant's Claim 1.

Second, Pereira fails to disclose a priority resolution circuit configured to hierarchically resolve *competing soft priorities* ***and*** *competing hard priorities* between two or more of the plurality of active hit signals having equivalent highest soft priorities, as recited in Applicant's Claim 1.

As mentioned above, Pereira fails to disclose a CAM device in which each CAM block has an arbitrarily assigned soft priority that is independent of the CAM array block's physical location relative to the other CAM array blocks, and therefore does NOT disclose a priority resolution circuit configured to hierarchically resolve competing

soft priorities. The Examiner points to col. 35, lines 13-28, which states:

> FIG. **46** shows priority encoder logic **4400** that is one embodiment of priority encoder logic **1112** of FIG. **13**. Priority encoder logic **4400** includes a row match circuit **4402** and a row priority encoder **4404** for each corresponding row of CAM cells **1122**. Each row mach circuit may be the same row match circuit **2402** of FIG. **26** that receives the match results from each of the match line segments M1-MZ of a corresponding row of CAM cells and, in response to the configuration information, generates a row match signal MR. Main priority encoder **4406** monitors the match results reflected on the Y row match signals MR(**0**)-MR(Y−1)and generates a row match address PRA that has $\log_2 Y$ address bits. The row address corresponds to the address of the highest priority row of CAM cells **1122** that has a row segment or a group of row segments that stores data that matches the comparand data for a given configuration.

There is no language in the above-referenced portion of Pereira that discloses a priority resolution circuit configured to *hierarchically resolve competing soft priorities and competing hard priorities* between two or more of the plurality of active hit signals having equivalent highest soft priorities, as recited in Applicant's Claim 1.

Accordingly, because Pereira fails to disclose or suggest either of the elements recited in Applicant's Claim 1, Claim 1 is patentable over Pereira.

Claims 3-5, 7, 9-14, and 59-60 depend from Claim 1 and therefore distinguish over the cited references for at least the same reasons as Claim 1.

Independent Claim 19

Applicant's Claim 19 is amended to recite, in part:

> wherein the priority resolution circuit is configured to resolve the competing soft priorities for all possible combinations of soft priority order between the plurality of active hit signals, wherein each hard priority is a unique value indicative of the corresponding CAM array block's physical location relative to the other CAM array blocks, and each soft priority is an arbitrarily assigned value that is independent of the corresponding CAM array block's physical location

As discussed above with respect to Claim 1, Pereira fails to disclose or suggest that each CAM block has an *arbitrarily assigned soft priority that is independent* of the CAM array block's physical location relative to the other CAM array blocks, and also fails to disclose a priority resolution circuit that is configured to *resolve competing soft priorities and competing hard priorities* when the soft priorities of multiple active signals are equivalent. Accordingly, Pereira fails to disclose or suggest the above-recited element of Claim 19, and therefore Claim 19 is patentable over Pereira.

Claims 20-21 depend from Claim 19 and therefore distinguish over the cited references for at least the same reasons as Claim 19.

Independent Claim 22

Applicant's Claim 22 is amended to recite:

> A content addressable memory (CAM) device, comprising:
>
> a plurality of CAM array blocks each including a plurality of rows of CAM cells, wherein each CAM array block has a unique hard priority indicative of the CAM array block's physical location relative to the other CAM array blocks, and has an arbitrarily assigned soft priority that is independent of the CAM array block's hard priority;
>
> means for identifying a highest priority one of said plurality of CAM array blocks having respective matching entries therein during a search operation, by evaluating the soft priorities of said plurality of CAM array blocks according to numeric significance so that matching entries in a first of said plurality of CAM array blocks are treated as having higher priority than matching entries in a second of said

plurality of CAM array blocks when the soft priority of the first of said plurality of CAM array blocks is higher than the soft priority of the second of said plurality of CAM array blocks and vice versa when the soft priority of the second of said plurality of CAM array blocks is higher than the soft priority of the first of said plurality of CAM array blocks

The arguments made above with respect to Claim 1 are equally applicable to Claim 22, and therefore Claim 22 is patentable over Pereira for reasons similar to those of Claim 1.

Independent Claim 23

Applicant's Claim 23 is amended to recite, in part:

after completion of said evaluating soft priorities, evaluating competing hard priorities between at least two of the plurality of CAM array blocks having the same soft priorities, wherein each hard priority is a unique value indicative of the corresponding CAM array block's physical location relative to the other CAM array blocks, and each soft priority is an arbitrarily assigned value that is independent of the corresponding CAM array block's physical location

The arguments made above with respect to Claim 19 are equally applicable to Claim 23, and therefore Claim 23 is patentable over Pereira for reasons similar to those of Claim 19.

Independent Claim 24

Applicant's Claim 24 is amended to recite, in part:

a priority resolution circuit configured to resolve competing soft priorities for all possible combinations of soft priority order between said plurality of CAM array blocks and further configured to resolve competing hard priorities between at least two of said plurality of CAM array blocks having the same soft priority, during an operation to search the plurality of CAM array blocks to identify respective matching entries therein, wherein each hard priority is a unique value indicative of the corresponding CAM array block's physical location

relative to the other CAM array blocks, and each soft priority is an arbitrarily assigned value that is independent of the corresponding CAM array block's physical location

The arguments made above with respect to Claim 19 are equally applicable to Claim 24, and therefore Claim 24 is patentable over Pereira for reasons similar to those of Claim 19.

Claims 25-28 depend from Claim 24 and therefore distinguish over the cited references for at least the same reasons as Claim 24.

CONCLUSION

In light of the above remarks, it is believed that Claims 1, 3-5, 7, 9-14, 19-28, and 59-60 are in condition for allowance and, therefore, a Notice of Allowance of Claims 1, 3-5, 7, 9-14, 19-28, and 59-60 is respectfully requested. If the Examiner's next action is other than allowance as requested, the Examiner is requested to call the undersigned at (408) 236-6646.

Respectfully submitted,

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Dated

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